FULLY INTEGRATED ALL-CMOS AM TRANSMITTER WITH AUTOMATIC ANTENNA TUNING

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Cross-Reference to Related Applications

This application is a continuation-in-part of application serial no. 09/074,997, filed on May 8, 1998, entitled "Fully Integrated All-CMOS AM Transmitter with Automatic Antenna Tuning," which is based on the provisional application serial no. 60/046,128, filed May 9, 1997, entitled "Fully Integrated All-CMOS AM Transmitter With Automatic Antenna Tuning", by J. Scott Elder, Joseph T. Yestrebsky, and Mohammed D. Islam.

BACKGROUND

Field of the Invention

This invention relates to transmitters and, in particular, to an integrated transmitter with automatic antenna tuning.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1a is a block diagram illustrating the functional units in a transmitter in accordance with one embodiment of the invention.

Figure 1b identifies pins of an integrated circuit incorporating the transmitter shown in Figure 1a.

Figure 2a shows a block diagram illustrating the functional units in a transmitter in accordance with a second embodiment of the invention.

Figure 2b identifies pins of an integrated circuit incorporating the transmitter shown in Figure 2a.

Figure 3a shows a block diagram of an example of a reference oscillator.

Figure 3b shows a block diagram of an example Filter Tune circuit.

Figure 4 shows a block diagram of an integrated transmitter according to the present invention.

Figures 5a through 5j show block diagrams and circuit diagrams of the antenna tuning portion of a transmitter according to the present invention.

In the figures, elements having similar functionality are identically labeled.

DETAILED DESCRIPTION

The Embodiments of Figures 1a and 1b

Figure 1a illustrates the basic structure and elements of one embodiment of a transmitter according to the present invention. The elements can be constructed on a single semiconductor Chip using Complementary Metal Oxide Semiconductor (CMOS) technology. Other bipolar type elements, for example diodes and transistors, can also be constructed in CMOS technology, where appropriate. The block diagram shown in Figure 1a includes the following elements, with associated reference numbers:

Functional Element		Reference No.
a.	Reference Oscillator	1
b.	Phase Detector	2
c.	Loop Filter	3
d.	Filter Tune	3a
e.	Track and Hold	4
f.	Differential Oscillator	5
g.	Prescaler	5a
h.	Div_M	6
i.	Varactor Charge Pump	7a
j.	Charge Pump	7b
k.	Bandgap Reference	8

In the embodiment of Figure 1a, the elements of the transmitter are fully integrated, i.e., all of these functions are, in their entirety, simultaneously incorporated onto a single semiconductor die (integrated circuit or IC). Aside from power supply decoupling capacitors, no external components are included for operating the transmitter except an antenna (L1, L2), and antenna resonating capacitor (C1). Additional aspects of the invention (to be detailed subsequently) reduce overall transmitter system complexity and cost, while improving transmitter performance.

Special Charge Pump circuitry 7b can be included within the embodiment to allow for applications which use a wide range of supply voltages. This makes the embodiment shown in Figure 1a quite general in nature, and lowers overall radio system costs. In most embodiments of charge pump 7b, nFETs are cascaded to guarantee that nFET drain-to-source voltage is clamped to acceptable levels, thus protecting the nFET devices

from hot-electron effects in applications with large
external supply voltages.

Reference Oscillator 1 generates a precise timing
waveform based on a timing element or timing signal
5 applied externally at the reference input pad 30 of the
embodiment shown in Figure 1a.

Phase Detector 2, Loop Filter 3, Filter Tune 3a,
Differential Oscillator 5, Prescaler 5a and divide-by M
circuit 6 collectively form a phase-locked loop (PLL)
10 where the frequency of Differential Oscillator 5 is
locked to that of Reference Oscillator 1.

Filter Tune 3a can itself be a phase-locked loop
tuned to the Reference Oscillator 1. Filter Tune 3a
generates a bias current I_{bias} for Loop Filter 3. This
15 approach stabilizes the performance characteristics of
Loop Filter 3 against semiconductor process variation
during chip production and temperature variations
during operation of the chip.

Differential Oscillator 5 serves as the source of
20 the transmit frequency. It is important to note that
oscillator 5 is within the phase-locked loop of phase
detector 2, loop filter 3, prescaler 5a, and divide-by
M circuit 6 and includes a voltage controlled
oscillator (VCO). Oscillator tuning can be
25 accomplished by means of a differential structure of
diffusion type p-n diodes (varactor diodes) within
differential oscillator 5. Some embodiments may
alternatively include tuning diodes external to the
integrated circuit and connected in a differential
30 manner. Some embodiments may alternatively include a
phase detector and up/down converter coupled to an
array of tuning capacitors.

Differential oscillator 5 provides a differential
output into a (differential) antenna L1, L2. The

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antenna formed by L1 and L2 is coarsely tuned by
capacitor C1, and fine tuned to the frequency of
Reference oscillator 1 via the tuning structure of
differential oscillator 5. L1, L2, and C1 can be

5   externally applied to the integrated circuit shown in
Figure 1a at pads 31 and 32. For less demanding
applications, where harmonic distortion is less
important, differential oscillator 5 need not be
differential in nature and only a single-ended

10   oscillator can be utilized, which reduces IC pin count.
        Addition of external resistor R_{bias} coupled to pad
33 in Figure 1a sets a bias current in differential
oscillator 5, which in turn sets the transmit power
level. For fixed transmit power applications, this

15   bias may be fixed on the integrated circuit itself,
eliminating the need for pad 33.
        In the embodiment shown in Figure 1a, the output
signal from differential oscillator 5 is frequency
divided by prescaller 5a and divide-by M circuit 6.

20   Prescaller 5a and divide-by-M circuit 6 output a signal
with frequency near that of reference oscillator 1,
within the locking and tracking range of the phase-
locked loop that includes differential oscillator 5.
        In some embodiments, a charge pump 7b provides

25   voltage multiplication, which allows the integrated
circuit to operate with supply voltages below 3V. An
externally applied pumping capacitor C_{FLY} is supplied
across pads 36 and 37. This supply voltage generation
technique can either be open loop controlled or closed

30   loop controlled. In a closed loop application, the
operation of charge pump 7b ceases when the external
supply voltage is sufficient for proper operation of
the transmitter. In an open loop application, the
voltage settles to an integer multiple of the input

voltage source. The embodiment of Figure 1a is capable of operating with an external supply voltage VDD to pads 35 that can be greater than about 12V. The operating voltage VBB of the integrated chips is

5 supplied at pad 34.

Track and hold circuit 4 holds the output voltage of loop filter 3 constant during transmit 'spaces', when differential oscillator 5 is disabled. This function requires an externally applied hold capacitor

10 C_H on pad 38. An alternative embodiment includes a hold capacitance C_H integrated on the IC Chip (e.g., a DAC approach).

The operation of track and hold circuit 4 and differential oscillator 5 is controlled by the data

15 input signal at pad 39. During "space" signals, differential oscillator 5 is off (i.e., not transmitting) and track and hold 4 holds the output voltage of loop filter 3 constant. During "mark" signals, track and hold 4 outputs the signal from loop

20 filter 3 and differential oscillator 5 is on (i.e., transmitting). Some embodiments include a data encoder circuit 40 that inputs a data signal from pad 39 and encodes it for transmission. Transmission is accomplished by controlling the output power of

25 differential oscillator 5. The output signal to antenna L1, L2 can be modified for any data transmission scheme.

A bandgap reference circuit 8 provides temperature and supply voltage compensated bias voltages and

30 currents for critical nodes within the invention.

The embodiment of Figure 1a allows for packaging in a 10 pin package. Embodiments can also have a fewer or greater number of pins. For example, in applications where charge pump 7b is not required (i.e.

adequate supply voltage exists for proper device operation), embodiments with fewer pins are possible.

Numerous physical embodiments of the invention exist, depending on the intended applications and

5   system requirements. An embodiment of an integrated circuit is illustrated in Figure 2b, along with those signals which are required for the embodiment shown in Figure 1a. Some signals which depend on the application, system requirements, and level of

10   integration are also shown. One need not, for example, integrate charge pump 7b onto the integrated circuit. Charge pump 7b can be provided external to the IC chip shown in Figure 1b. Removal of charge pump 7b from the integrated circuit may be more desirable than the more

15   highly integrated transmitter in some applications.

Having said this, Figure 1b illustrates an embodiment of the invention having a 5-pin IC package. The 5-pin IC package includes pads 35(VDD), 30 (VREFIN), 41 (VSS), 31 (ANTI) and data (39). Placing

20   further functions (e.g. an integrated circuit with charge pump 7b or data encoder 40) on the IC package may result in additional pins. A particular embodiment of the invention can include any number of pins greater than 5. Additionally, particular embodiments of the

25   invention can be packaged in any fashion. Packaging technologies are well known to one skilled in the art. Additionally, implementation of embodiments of the invention to CMOS technologies (i.e., forming particular elements on semiconductor chips) is well

30   known in the art.

The embodiments of the invention shown in Figure 1a converts an input (logic level) data sequence on pin 39 into an amplitude modulated (AM) or frequency modulated (FM) RF carrier. Transmit antenna L1 and L2

(Figure 1a) forms part of the resonant network of Differential (RF) Oscillator 5. Differential Oscillator 5 is enclosed within a closed-loop control system (a phased-locked loop) at the frequency of reference

5   oscillator 1. The antenna L1 and L2 are combined with variations in differential oscillator 5 to form an LC resonant circuit, which has a resonance point that is automatically tuned to the transmit frequency. The transmit frequency can be an integer multiple of the

10   output frequency of reference oscillator 1.

Two Charge Pumps, pumps 7a and 7b, and appropriate control functions are included in the transmitter of Figure 1a to (1) provide sufficient bias voltage for varactor diodes, and (2) allow the integrated circuit

15   to function properly for externally applied bias supplies below about 3V.

Reference Oscillator 1

Reference Oscillator 1 develops the precision

20   timing signal which is used by the phase-locked loop to set the transmit frequency. The phase-locked loop includes phase detector 2, loop filter 3, track and hold 4, differential oscillator 5, prescalar 5a, and divide-by-M circuit 6. In most embodiments, Reference

25   Oscillator 1 is of the Colpitts variety, and is connected to a timing device external to the integrated circuit (IC). Typical timing devices include ceramic resonators, crystals, or (tuned) inductor-capacitor tank circuits. Phase lag capacitors generally

30   associated with ceramic resonators are integrated onto the IC to lower cost.

In most embodiments, as shown in Figure 3a, reference oscillator 1 includes a single-ended amplifier 101 which provides differential outputs. In

some embodiments, amplifier 101 provides no dc gain, eliminating any dc offset correction requirements. The amplifier output signal is differentially coupled into a comparator 102 which limits the output signal

5   waveform to logic level swings. The output stage of comparator 102 is ac current balanced to eliminate any unnecessary power supply noise. Reference oscillator 1 requires only a single IC pin for connection of the precision timing element or signal input to amplifier

10 101.

Finally, reference oscillator 1 supports the application of an external (precision) timing signal rather than a timing element. The timing signal is applied at the same terminal as would receive an

15 external timing element signal.

Phase Detector 2

Phase detector 2 provides a measure of the frequency difference between the output signal from

20 Reference oscillator 1 and the output signal from differential oscillator 5, frequency divided by scale factor M within Div_M circuit 6 and prescaled in prescaler 5a. Phase detector 2 needs only to discriminate frequency differences because phase error

25 in the phase-locked loop (PLL) does not affect performance of the transmitter.

In most embodiments, phase detector 2 is a digital phase-frequency detector. Digital phase-frequency detectors are advantageous for at least two reasons:

30 Firstly, the circuit output signal is differential in nature; secondly, when the phase-locked loop finally acquires frequency and phase lock, phase-frequency detector 2 outputs a series of very narrow pulses in the time domain, which is much easier to filter with an

integrated loop filter than a phase detector that
exhibits quadrature phase lock.

Loop Filter 3 and Filter Tune 3a

5   The output waveform of phase detector 2 contains
both a dc and an ac term; the dc term represents the
frequency error between the output signal of reference
oscillator 1 and the output signal of differential
oscillator 5 prescaled and divided by scale factor M.

10   Only the dc term is of value; the ac term is removed by
loop filter 3.

In many embodiments, loop filter 3 is a gm-c type
filter, a gm-c type filter is advantageous for at least
three reasons. Firstly, the variance in gm-c filter

15   characteristics is almost completely related to the gm
variances since integrated capacitors are well behaved.
Secondly, a fairly high order filter may be constructed
using only modest amounts of integrated capacitance,
which reduces the cost of producing the integrated

20   circuit chip. Thirdly, such filters are easily 'tuned'
to stabilize their characteristics against
semiconductor process and temperature variations. Such
tuning is provided from a tuning phase-locked loop,
filter tune 3a, 'slaved' from reference oscillator 1.

25   An embodiment of filter 3a is shown in Figure 3b.
Filter Tune 3a is itself a phase-locked loop,
referenced to the frequency of the output signal from
reference oscillator 1. The phased-locked loop of
filter tune 3a may include a phase detector 300,

30   current controlled oscillator 301, prescaler 302, and
divided-by M circuit 303. The phase-locked loop of
filter tune 3a adjusts the bias current of the current-
controlled oscillator of filter tune 3a to force the
current-controlled oscillator frequency to equal the

frequency of the output signal from reference
oscillator 1. This may be accomplished directly or
indirectly through the use of frequency prescalers 302
or frequency dividers 303. The resultant bias current

5   is mirrored in current mirror 304 to provide the bias
current for loop filter 3.

Track and Hold 4

During transmission of 'spaces', differential

10   oscillator 5 may be disabled. This 'breaks' the phase-
locked loop that includes phase detector 2 and
differential oscillator 5. Track and hold 4 is used to
hold the state of the phase-locked loop to that just
prior to disabling differential oscillator 5,

15   signifying a 'space' transmission. This is desirable
for at least two reasons: (1) so that the phase-locked
loop does not have to require frequency lock for each
'mark' transmission; and (2) to assure that
differential oscillator 5 is not 'chipped' or swept in

20   frequency as the Phase-locked loop settles out during a
'mark' transmission.

The data signal input to track and hold 4, which
is the output signal from data encoder 40, controls
track vs. hold operation. During 'space'

25   transmissions, track and hold 4 is placed in the hold
mode.

Some applications may be better served (e.g., be
of lower cost for the transmitters) by the use of an
external hold capacitor (C_H) for track and hold 4, as

30   shown in Figure 1a. However, the effective hold
capacitance can be integrated onto the IC chip, with
additional cost, and perhaps a modest compromise in the
'droop' of the hold voltage. For example, to support
very low data rates, an external hold capacitor into

the integrated circuit is preferred, but as the operational data rate increases, the impact of integrating this capacitor into the integrated circuit is less deleterious to cost and performance. So, an

5   alternative embodiment is the integration of C_H, which reduces the IC pin count of the resulting integrated circuit by one.

Differential Oscillator 5

10   Differential oscillator 5 includes a voltage controlled oscillator (VCO). The voltage controlled oscillator can be based on two cross-coupled Field Effect Transistors (FET's) where antenna L1 and L2 serves as the load impedance for the FET's. The cross-

15   coupled FET structure provides the feedback for oscillatory behavior. In the embodiment shown in Fig. 1a, the antenna is applied externally to the integrated circuit, differentially coupled to the external bias supply. In Fig. 1a, antenna L1, L2 is coupled to pads

20   31 and 32, respectively. The differential antenna is shown in Figure 1a as components L1 and L2. The antenna is brought coarsely in the range of the proper transmit frequency by coupling an external capacitor C1 across the external (differential) antenna, as is

25   illustrated in Figure 1a. This sets the nominal frequency of oscillation for differential oscillator 5. This coarse capacitor can also be integrated onto the integrated circuit, further reducing external component requirements. By integrating the coarse capacitance on

30   the integrated circuit chip, the antenna design requirements are further restricted so that a resonant frequency of the antenna and capacitor circuit is near to the operating frequency of differential oscillator 5.

The differential oscillator frequency is
adjustable via a dc control signal VAFC, which is the
filtered output signal from phase detector 2.   Two
reverse-biased p-n diffused-junctions (varactors) are

5   connected differentially across the cross-coupled FET's
of differential oscillator 5.   As the dc level of VAFC
varies, the capacitance of the reverse-biased p-n
junctions varies inversely.   This capacitance forms
part of the resonant tank circuit which sets the

10   frequency of oscillation.   Thus, a differential
varactor diode approach can be the method used to
modify the resonant point of antenna L1, L2.   An
alternative varactor approach is to use the CV
characteristics available in an MOS diode.

15   A bias current for differential oscillator 5 is
set via addition of resistor Rbias, shown externally to
the embodiment of Figure 1a.   A closed-loop voltage
follower regulates a voltage based on the internal
bandgap reference 8 on the integrated circuit.   Rbias

20   sets the bias current based on the regulated voltage;
this current is mirrored to differential oscillator 5
as the bias current.

        An alternative to providing R_{bias} externally is to
integrate this onto the chip as a fixed, unmodifiable

25   current.   This will result in a fixed, unmodifiable
transmit power level.   If the on-chip R_{bias} resistor is
replaced by a digital to analog converter, the transmit
power level can be varied by communicating to the
integrated circuit (via separate input pins) a data

30   pattern that sets the desired transmit power level.

        Input data is used to electronically steer the
bias current to differential oscillator 5.   During
'mark' transmissions, the bias current is connected to
differential oscillator 5.   Differential oscillator 5

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then begins to oscillate, transmitting an RF carder during the 'mark' interval. Alternatively, during a 'space', the bias current is disconnected from differential oscillator 5, and so oscillation ceases,

5   transmitting the equivalent of a 'space'.

Special back-to-back trapped drain field effect transistor (FET) structures can be employed at critical high frequency nodes of differential oscillator 5 to minimize capacitance and improve bandwidth. The

10   preferred embodiment is circular drain structures, although other structures (octagonal, hexagonal, etc.) are acceptable. This structure has important ramifications, since the result is a very small parasitic capacitance at the drain node of the FET and

15   a larger capacitance at the source node of the FET. This 'breaking-apart' of the normally equal drain and source parasitic capacitances actually further improves the gain-bandwidth (GBW) of differential oscillator 5 beyond just the improvement anticipated by a lowering

20   of the drain capacitance. Said another way, the extra source capacitance actually improves GBW.

A differential oscillator such as differential oscillator 5 is employed for a good reason, namely that such a structure driving a differential antenna results

25   in reduced harmonic distortion of the transmitted signal. This is important in some critical applications, but is less important in other applications. Thus an alternative embodiment is the use of a non-differential oscillator where application

30   requirements permit. This reduces the cost of the transmitter, as well as its pin count. It is anticipated that a differential scheme will be necessary to meet most international regulatory

requirements similar to the United States FCC and Part 15 of the Code of Federal Regulations.

Prescaler 5a

5   Differential oscillator 5 operates at a very high frequency, beyond the operating range of conventional CMOS logic dividers. This frequency is divided down by a high speed circuit, prescaler 5a, before further division by conventional logic can take place. One
10 embodiment of prescaler 5a is composed of a concentration of high speed cross-coupled FET divide-by-two circuits.

Prescaler 5a is biased using a current which is tuned to reference oscillator 1. This guarantees that
15 the bandwidth of prescalar 5a is temperature and process independent.

Special back-to-back trapped drain field effect transistor (FET) structures can be employed at critical high frequency nodes of prescaler 5a to minimize
20 capacitance and improve bandwidth.

Div-M 6

Once the frequency of the output signal from differential oscillator 5 is prescaled to an
25 appropriate lower frequency, conventional CMOS logic dividers are used to further divide the frequency down to approximately the operating frequency of reference oscillator 1. This is accomplished by division function Div_M 6 (divide by M circuit).

30

Varactor Charge Pump 7a

The reverse-biased p-n junction capacitors (i.e., varactors) included in differential oscillator 5 require a large bias potential for proper operation.

On the other hand, the varactors require very little bias current. The need for extra circuitry to construct the varactor bias voltage depends on the magnitude of the bias supply V_{DD} externally supplied to

5   the chip on pad 35.

For applications where the external bias supply is in the vicinity of 12V, extra bias generation circuitry is not required. However, for lower external bias voltages, a circuit is required to synthesize a larger

10   varactor bias voltage V_{BB} from the smaller external bias voltage V_{DD}. This function is preferentially accomplished by a voltage multiplying charge pump 7b, since the load current is very small. Such a circuit in CMOS is easily integrated onto the chip without the

15   need for additional external components. Thus, no additional pins are required to provide this function on the integrated circuit chip.

Charge Pump 7b

20   Applications for this transmitter chip often demand operation with external bias supply voltages ranging from 12V down to below 3V. However, operation at bias voltages much below about 5V in CMOS is difficult without special processing (to lower FET

25   threshold voltages), and the use of sub-micron or deep-sub-micron technology in chip manufacturing technologies. To meet this requirement using inexpensive technology, a voltage multiplying charge pump 7b is included. Charge pump 7b provides supply

30   voltages of sufficient magnitude (generally greater than approximately 4V) from externally applied voltages lower than this value. The output voltage from charge pump 7b, V_{BB} is then used instead of the external bias

voltage V_{DD} to power-up other elements on the integrated circuit chip.

Charge pump 7b is different from varactor charge pump 7a. Firstly, charge pump 7b must supply much

5   larger output currents than varactor charge pump 7a. Secondly, varactor charge pump 7b is required for the transmitter to operate except in applications where the external supply voltage is approximately 12V. Charge pump 7b, however, is only required for applications

10   where the external supply voltage is below about 5V. Also, varactor charge pump 7a requires no external pins on the IC package. Charge pump 7b requires several package pins, (e.g., pads 36 and 37 for a pumping or 'flying' capacitor C_{fly}, and pad 34 for a filtering

15   capacitor C_F).

Thus, there are several physical embodiments of integrated circuits. It is perhaps most cost effective to include varactor charge pump 7a on any physical embodiment since this costs no package pins and only

20   modest CMOS die area. However the inclusion of charge pump 7b is expensive due both to die area and required package pins, and thus may not be included on embodiments intended for applications with greater than about 5V external supply voltages. One further

25   alternative is not to include charge pump 7a on the transmitter chip, but to provide this function externally, for sub-5V supply applications.

Bandgap Reference 8

30   A bandgap reference circuit 8 is included on the chip of Figure 1a. The purpose of this function is to generate reference voltages which are temperature and supply voltage stable. Stable reference voltages are

required to bias various critical nodes within the transmitter chip.

5

The Embodiments of Figures 2a and 2b

Figure 2a shows a second embodiment of the invention. Transmitter 10 of Figure 2a includes the following elements:

Reference Oscillator	1;
Phase Detector	2;
Loop Filter	3;
Filter Tune	3a;
Track and hold circuit	4;
Differential Oscillator	5;
Prescalar	5a;
Divide by M circuit	6;
Varactor Charge Pump	7a; and
Bandgap Reference	8.

Most of these components have been discussed above and, therefore, they will not be further discussed in detail here. Differential oscillator 5 of the embodiment shown in Figure 2a includes the following elements:

Voltage Controlled Oscillator	11;
Buffers	12 and 14;
Power Amplifier	13;
Antenna Tuning Circuit	15;
Tuning Array	16; and
Power Controller	17.

Differential oscillator 5, as shown in the embodiment of transmitter 10 shown in Figure 2a, is

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coupled with a loop antenna 20, rather than a differential antenna L1, L2 as shown in Figure 1a.

Differential oscillator 5 includes voltage controlled oscillator 11. Voltage controlled

5   oscillator 11 forms a phase-locked loop with prescalar 5a, divide-by M circuit 6, phase detector 2, and loop filter 3, as has been discussed above. Track and hold 4 holds the output signal from loop filter 3 constant during transmit spaces, when the differential

10 oscillator 5 is disabled from transmitting. Some embodiments of the invention omit track and hold 4, especially those with more complex modulation schemes. Due to the phase-locked loop, the output signal from voltage controlled oscillator 11 is at a frequency that

15 is set by the frequency of the input signal at the reference-in pad 30 of the integrated circuit chip.

As was previously discussed, and shown in Fig. 3b, prescalar 5a outputs a signal of reduced frequency from that of voltage controlled oscillator 11. Divide-by M

20 circuit 6 outputs a signal having a frequency divided by a factor M from that of the output signal from prescalar 5a. Phase detector 2 compares the frequency of the signal outputted by divide-by M circuit 6 with that from reference oscillator 1. The output signal

25 from phase detector 2, filtered by loop filter 3, is input to voltage controlled oscillator 11 in order to control the frequency of the output signal from voltage controlled oscillator 11.

As was previously discussed, filter tune 3a

30 includes a phase-locked loop tuned to the frequency of reference oscillator 1. Filter tune 3a generates a bias current for loop filter 3 and stabilizes the performance of loop filter 3 against variations due to semiconductor processing and operating temperatures.

Voltage controlled oscillator 11 generates two differential signals, I and Q, which are quadrature in phase. The in-phase signal I is output from differential oscillator 5 to prescalar 5a. The in-

5　phase signal I is also input, through buffer 12, to power amplifier 13. Power amplifier 13 provides the output signal that drives antenna 20.

The quadrature signal Q is provided, through buffer 14, to antenna tune circuit 15. Antenna tune

10　circuit 15 adjusts the resonant frequency of the LC circuit formed by antenna 20 and tuning array 16 to correspond with the frequency of the output signals from voltage controlled oscillator 11. Tuning array 16 can, for example, include differential varactors 16a

15　and 16b. Differential varactors 16a and 16b can be continuously variable varactors or discrete varactors which include a switched capacitor array. Varactors 16a and 16b provide a desired amount of capacittance to tune antenna 20 to the operating frequency of VCO 11.

20　Power amplifier 13 provides a differential output signal into antenna 20. The LC circuit, including antenna 20, is tuned such that a resonance frequency of the LC circuit matches the frequency of the differential output signal from power amplifier 13,

25　which is the same as the operating frequency of voltage controlled oscillator 11, by antenna tune circuit 15. Antenna tune circuit 15 compares the phase of the differential output signal to antenna 20 with the quadrature output signal Q from voltage controlled

30　oscillator 11 and varies the effective capacitance of tuning array 16.

In embodiments where tuning array 16 includes varactors 16a and 16b, varactors 16a and 16b can be operated in either full depletion mode or in

enhancement mode, thereby creating high quality (Q) on-chip MOS capacitors. As a result of the high quality MOS capacitors, it is possible to tune the LC circuit including external antenna 20 without degrading the

5   overall quality of the antenna network.

Power controller 17 provides a negative feedback closed loop built around antenna 20 in order to control and modulate the transmit power. In the embodiment shown in Figure 2a, power levels are controlled at AM

10   pad 42 by external resistors R1 and R2 while the data signal is input at ASK pad 39. Power controller 17 outputs a signal that controls the gain of power amplifier 13.

Power controller 17 is controlled by an AM voltage

15   signal input on pad 42. Data is input at pad 39. The data signal, shown here as an amplitude shift keyed (ASK) data sequence, is input to power controller 17. Power controller 17 modulates the output power of the transmitter in response to the data stream. In some

20   embodiments, power controller 17 may include a data encoder 40 (Fig. 1a). Embodiments of the invention can utilize any data transmission scheme (e.g., XDSL). Further, Power controller 17 may use frequency modulation instead of amplitude modulation by, for

25   example, modulating the control signal to varactors 16 or the control signal to VCO 11.

Figures 5a through 5j show block diagrams and circuit diagrams of portions of a transmitter according to the present invention. Figure 5a shows a block

30   diagram of the automatic tuning portion of transmitter 10. Voltage controlled oscillator 11, as shown in Figure 2a, is part of the phase-locked-loop formed by phase detector 2, loop filter 3, track-and-hold 4, VCO 11, prescalor 5a, and Div_M circuit 6. VCO 11 is

coupled to buffer 12 which is coupled to provide energy to loop antenna 20 at a transmit frequency set by VCO 11.

VCO 11 is also coupled, through buffer 14, to antenna tune 15. Antenna tune 15 controls capacitor tuning array 16 so that the resonant frequency of the circuit containing loop antenna 20 can be controlled by switching the capacitors of capacitor array 16 into the circuit. Antenna tune 15 includes phase detector 50 and up/down counter 51. Phase detector 50, compares the signals from VCO 11 with the signal from loop antenna 20 and adjusts the capacitance of capacitor array 16 by causing up/down counter 51 to be adjusted.

Figure 5b shows power controller 17 coupled to power amplifier 13. Power controller 17, as shown in Figure 5b, includes a forward gain GM amplifier 60, a summer 62, reference level 61, and full wave rectifier 63. The output signal from reference level 61, which depends on the AM signal, and the output signal from full wave rectifier 63, which depends on the signal from loop antenna 20, are summed in adder 62 and input to amplifier 60. The output signal from amplifier 60 determines the gain of power amplifier 13.

Figure 5c shows a block diagram of transmitter 10. PLL 71 inclues VCO 11, prescaler 5a, Div_M circuit 6, phase detector 2, loop filter 3, and track and hold 4. Amplitude control loop 70 includes power controller 17. Phase control loop 54 includes antenna tune 15 and capacitor array 16.

Figure 5d shows a circuit diagram of amplitude control loop 70. Loop 70 incudes amplifier 60 and a detector 64. A circuit diagram of the RMS detector of the antenna signal 64 is shown in Figure 5e. A circuit diagram of amplifier 60 is shown in Figure 5f. A

circuit diagram of power amplifier 13 is shown in Figure 5g.

A circuit diagram of phase detector 50 is shown in Figure 5h. Figure 5i shows a circuit diagram of phase

5   control loop 54, including up/down counter 51, phase detector 50, and capacitor array 16. In the circuit of Figure 5i, up/down counter 51 is formed from two counters 53. The circuit diagram for counters 53 is shown in Figure 5j.

10   In general, all of the above discussed components can be produced on a single integrated circuit with CMOS technology.

Alternative Embodiments and Enhancements

15   By implementing on a CMOS integrated Chip, it is economical to include encoder functions on the same IC since most of the applications for this type of radio transmitter include an encoder before the transmitter. The encoder can be either fixed or variable (i.e.,

20   programmable, like a microprocessor).

Other embodiments include the addition of a shutdown mode for low-power duty-cycling of the invention.

An encoder such as encoder 40 of Fig. 1a, may be

25   included in power controller 17, or between data input pad 39 and power controller 17. The encoder generates an on/off data stream which ultimately turns on/off a transmitter function.

The encoder on/off data stream can either be fixed

30   or variable. An example of a fixed data stream would be one permanently programmed in an encoder circuit with either switches or jumper connections. An example of a variable encoder data stream is one similar to that used in rolling code encoder systems. Rolling

code schemes are generally found in high security
applications where the user is trying to evade capture
of a valid encoder data stream for later broadcast to a
receiving decoder. Generally, these rolling code

5   encoder schemes embody erasable and reprogrammable
memory circuits. In that embodiments of this invention
now allow full integration of at least one embodiment
of a transmitter function, all of the encoder circuit
schemes can be integrated on one single silicon

10   integrated circuit at a very low cost.

In that embodiments of this invention are built on
a CMOS process technology, a microprocessor or similar
computing circuit element can be combined on the same
silicon integrated circuit with the invention since

15   modern low-cost microprocessors are almost always
constructed on a similar process.

The embodiments of the invention have certain
performance limits at the present time that are
expected to change in the future. One such limit is

20   the achievable upper operating frequency limit. One
skilled in the art will readily recognize that
embodiments disclosed here can continue to be scaled as
CMOS technology is scaled to continue applying the
invention at higher and higher operating frequencies.

25   The United States agency that regulates unlicensed
radio or RF transmitters, the FCC, has allocated
certain frequency bands and emission types for which
this type of device is intended. There are several
regulating bodies in other parts of the world which in

30   a similar manner control these same issues. In some
instances, the World's other regulatory agencies are
more restrictive in their operating rules than is the
FCC. Embodiments of this invention can be tailored for

operation under all of the various regulatory agency
provisions.

The primary application of this invention, but
certainly not the only application, is for automotive

5   keyless entry, garage door openers, home keyless entry,
security systems, and remote door bell ringers.
Obviously, there are numerous other applications that
combine a simple transmitter with a digital data stream
generation circuit. Figure 4 shows an embodiment of

10   the invention as a remote transmitter. Remote 70
includes battery 60, transmitter 10, antenna 20,
oscillator 50 and switch 55. In order to preserve
battery 60, R1 and R2 are as large as possible or
switched in order to draw current only when needed.

15   Oscillator 50 provides the reference input frequency
for reference oscillator 1(Fig. 2a).

This invention's uniqueness is further exemplified
by the observation that a complete RF radio
transmitting system can be built with no other external

20   RF components except an antenna.

While the embodiments specifically discussed here
illustrate an AM type transmitter, one skilled in the
art will recognize that an FM transmitter with
virtually the same circuit techniques described herein

25   can be built. The modifications that are necessary to
build FM transmission entail changing the phase-locked
loop division ratio or reference frequency by the
requisite frequency deviation for the system. This
will force the control system to tune the antenna

30   between any of a number of frequencies determined by
the phase-locked loop feedback divisor or reference
frequency values. In the limit, these values approach
infinity. A simpler FM modification is also possible
with the invention, namely varying the varactor diode

bias directly. This is a more traditional technique of FM modulation, although not previously implemented on CMOS silicon at the frequencies made possible by this invention.

5   As a result of the economy of scale associated with CMOS process technology, an extension of this invention is to build several transmitters on the same silicon die. This will allow one to build low-cost multi-channel systems which are either AM, FM, or

10   otherwise. A multi channel-channel system enhances the achievable data rate in much the same manner that increasing a digital systems data bus or address bus width.

        The embodiments described in this disclosure are

15   examples only and are not intended to be limiting. One skilled in the art will recognize obvious variations, each of which are intended to be within the scope and spirit of this invention. As such, the invention is limited only by the following claims.